IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Ishwardutt Parulkar et al.		
Assignee:	Sun Microsystems, Inc.		
Title:	ON-CHIP TESTING OF EMBEDDED MEMORIES USING ADDRESS SPACE IDENTIFIER BUS IN SPARC ARCHITECTURES		
Serial No.:	10/611,467	Filed:	June 30, 2003
Examiner:	Elmira Mehrmanesh	Group Art Unit:	2113
Docket No.:	P-8374		

Monterey, CA
August 30, 2006

Mail Stop Issue Fee
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF REPLACEMENT SHEETS OF DRAWINGS

Dear Sir:

The attached three (3) replacement sheets of drawings correct minor informalities and generally conform to USPTO drawing guidelines for Figs. 1, 2 and 3.

Sheet one, which includes Fig. 1, replaces the original sheet one including Fig. 1.

Sheet two, which includes Fig. 2, replaces the original sheet two including Fig. 2.

Sheet three, which includes Fig. 3, replaces the original sheet three including Fig. 3.

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If there are any questions concerning these replacement sheets, please call the undersigned at the number given.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 30, 2006.

Attorney for Applicant(s) — August 30, 2006 Date of Signature

Respectfully submitted,

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